

Figure 1

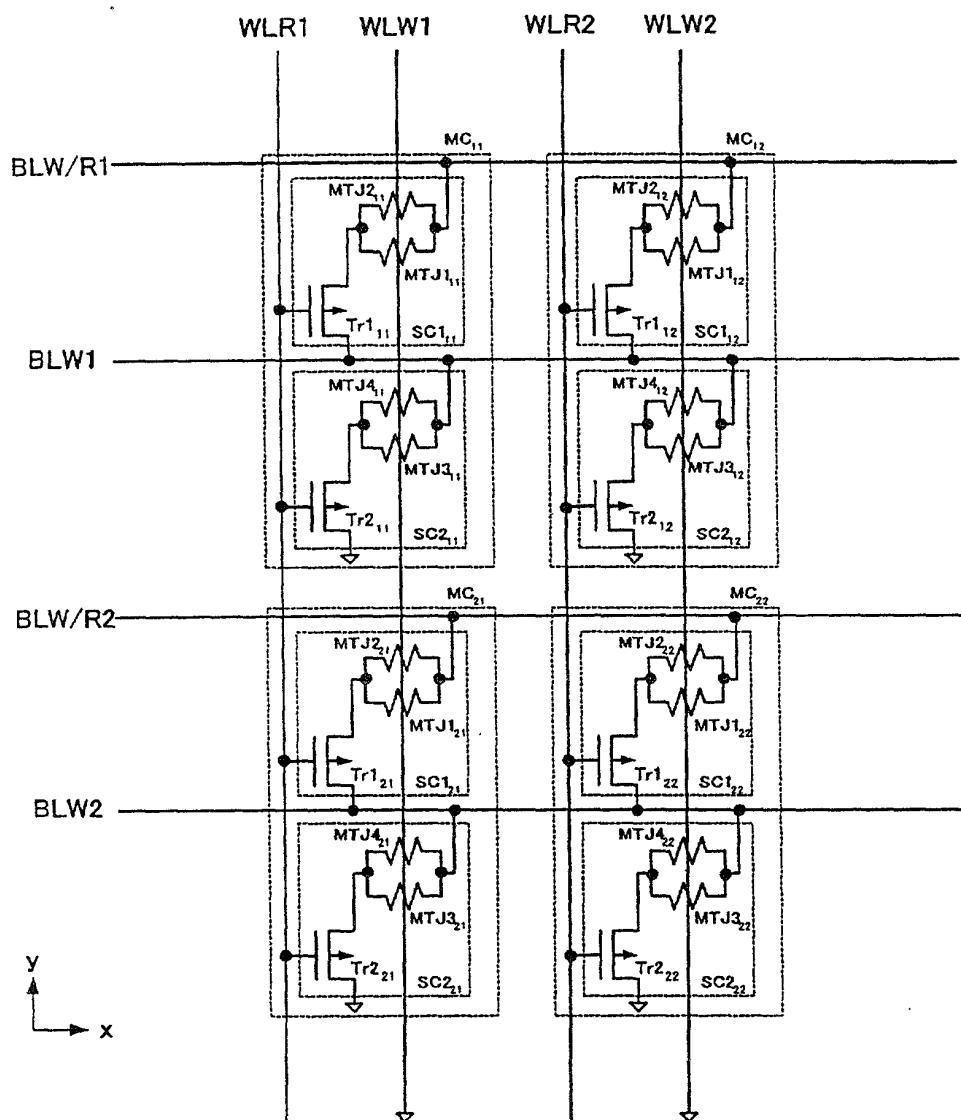


Figure 2 a

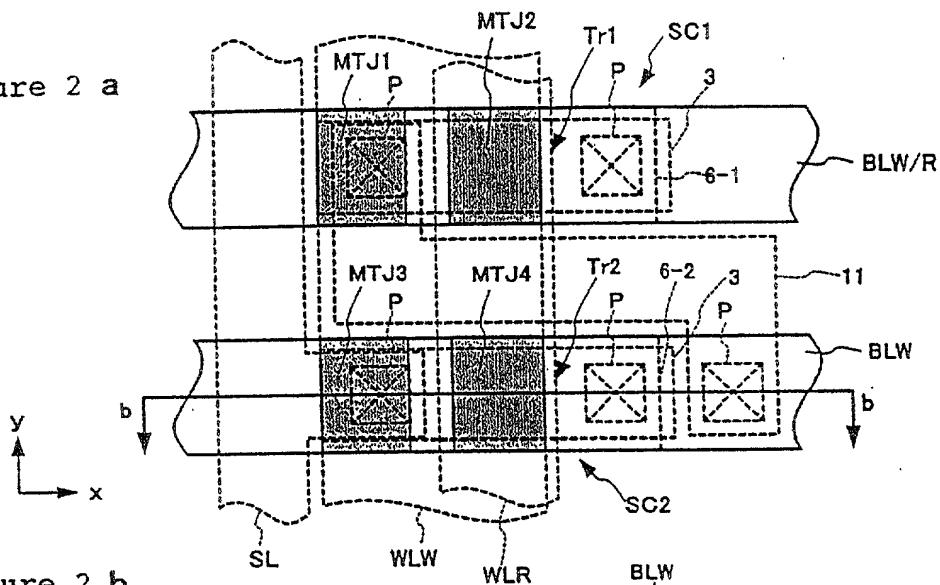


Figure 2 b

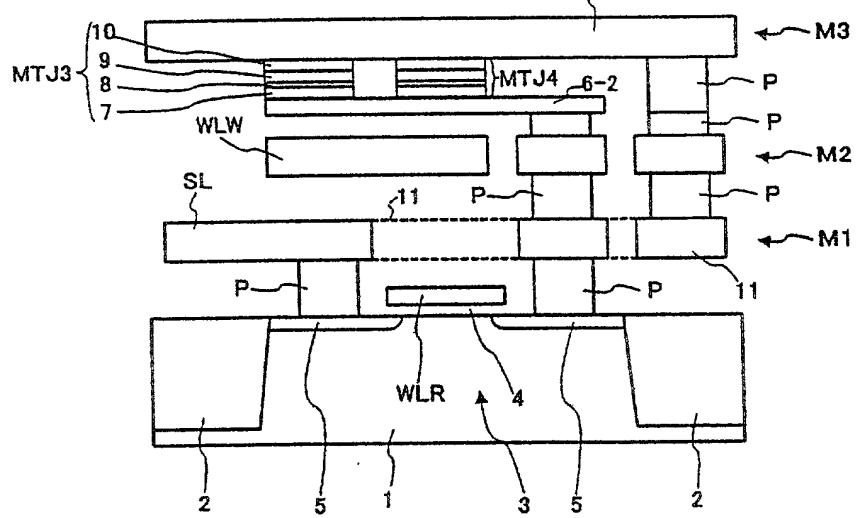


Figure 3

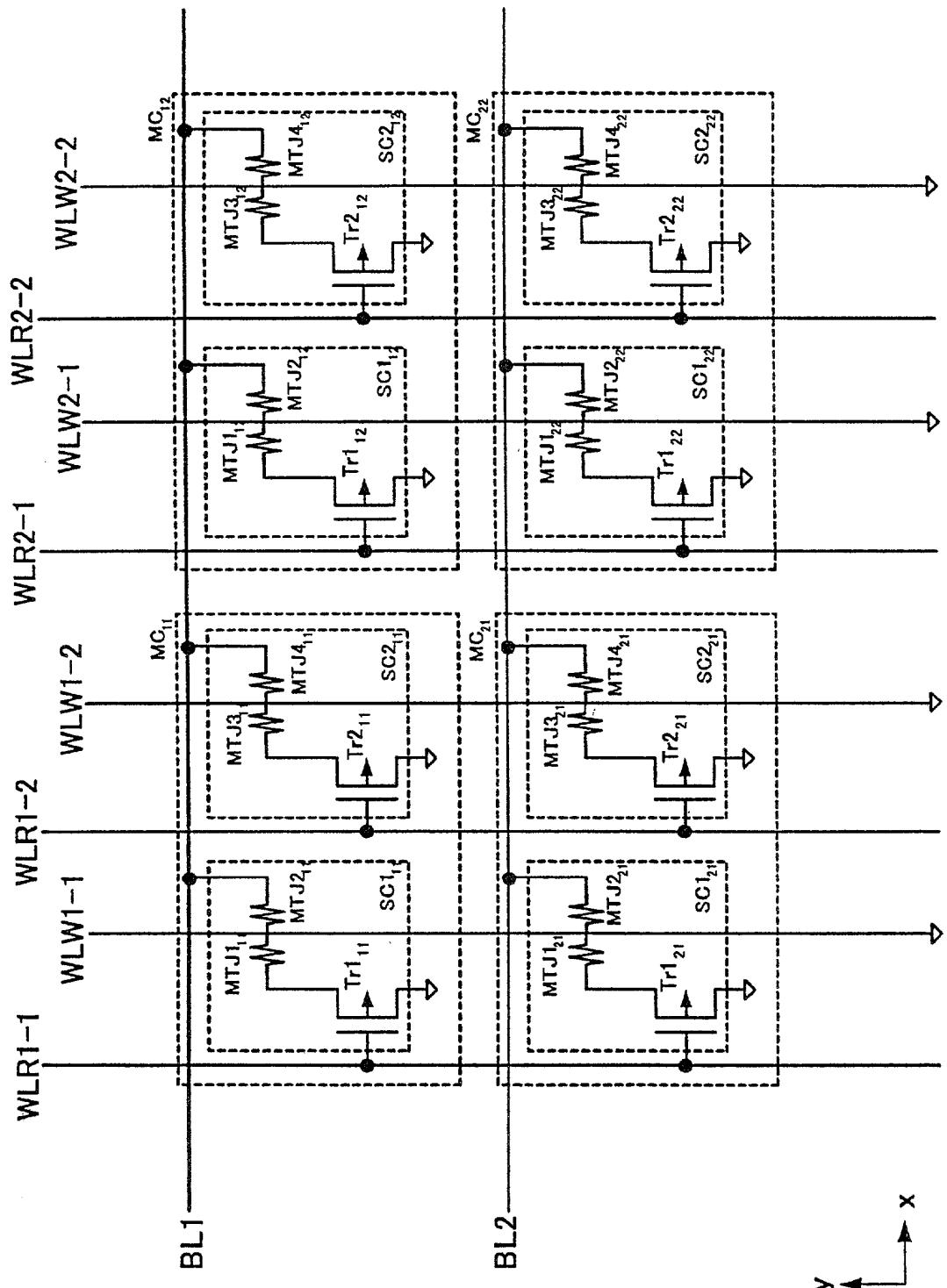


Figure 4

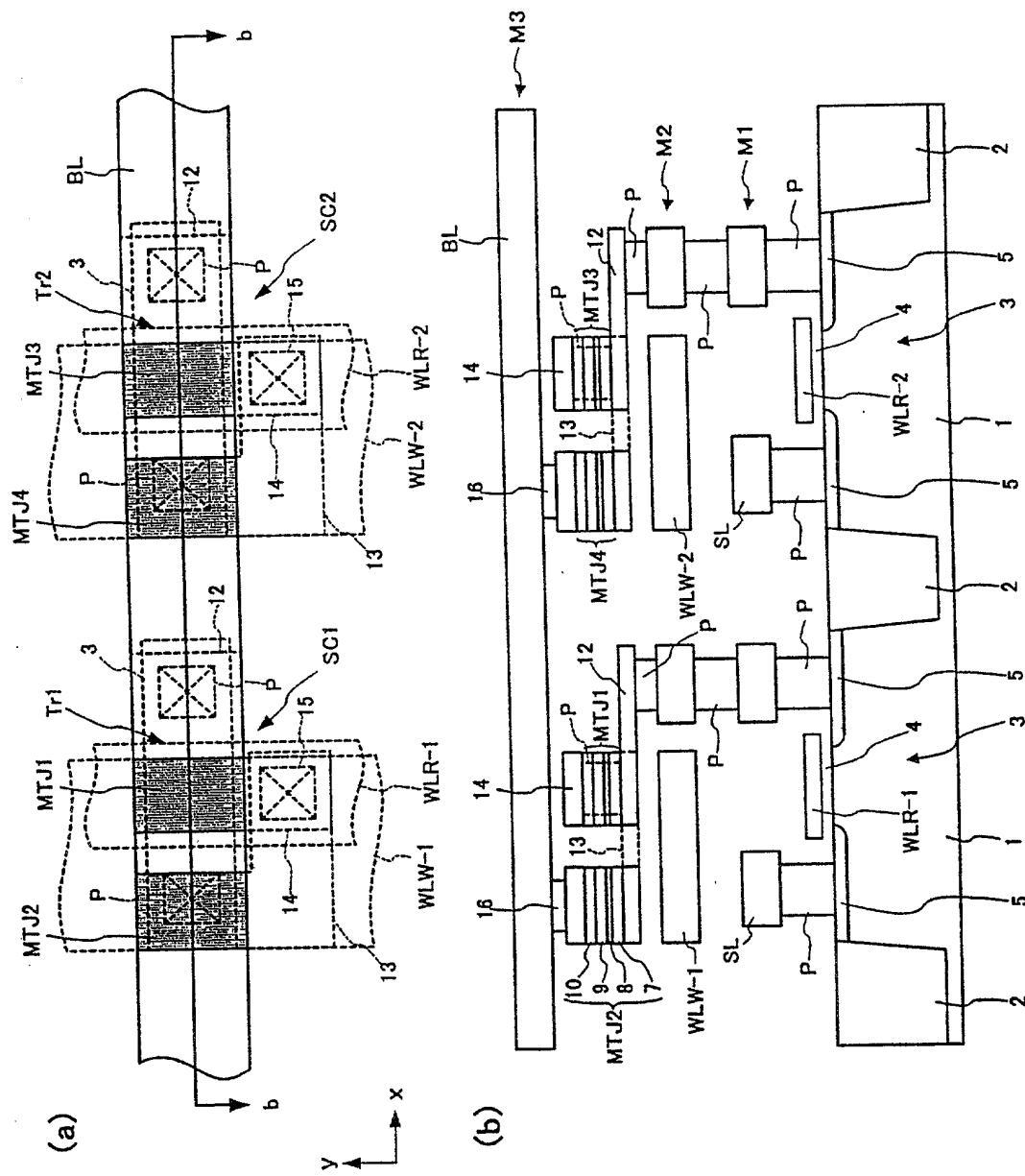


Figure 5

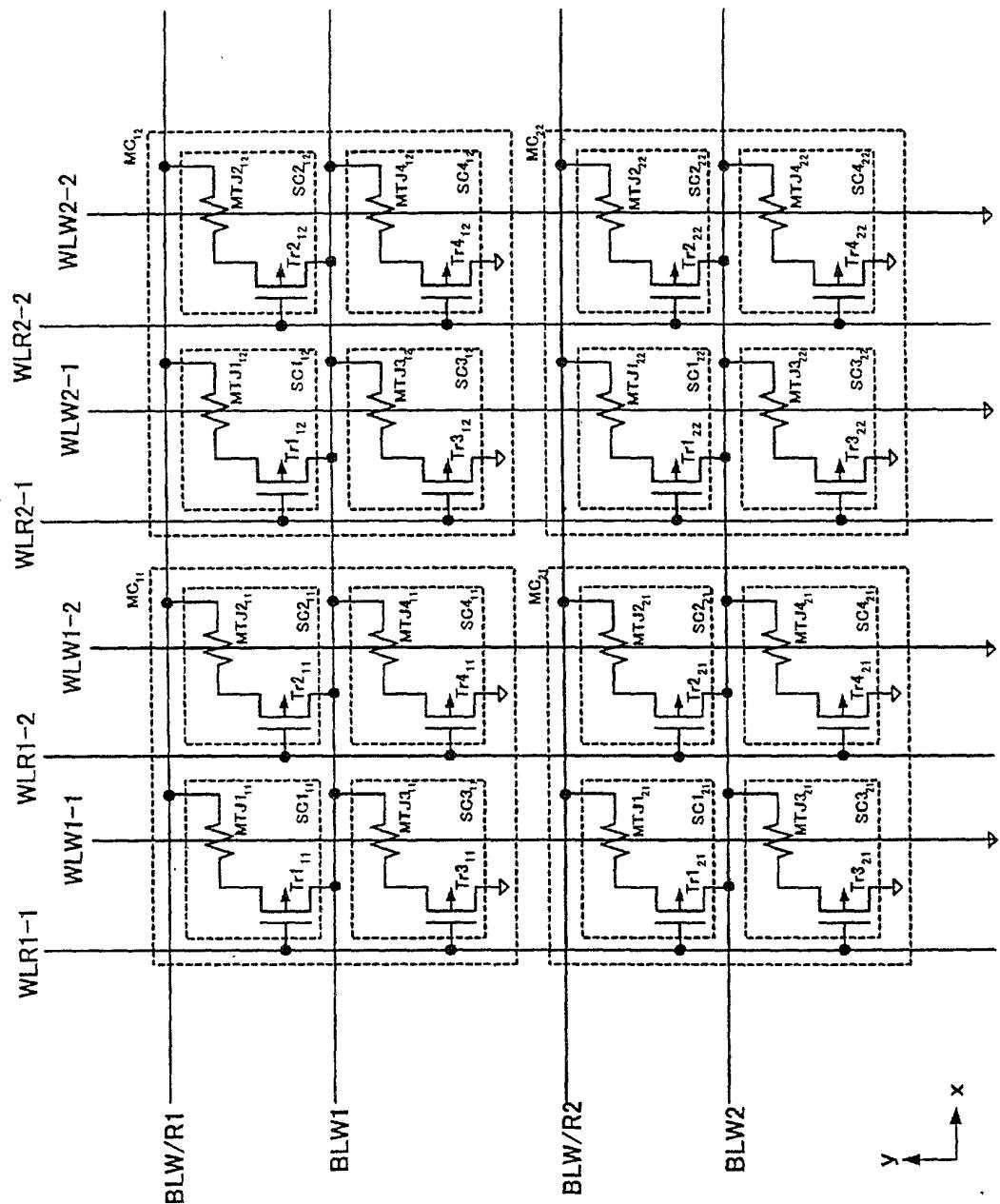


Figure 6
Figure 6 shows a cross-sectional diagram of a memory cell array. The array is organized into four columns labeled BL1, BL2, WLR1, and WLR2. The WLR1 and WLR2 columns represent word lines, while BL1 and BL2 represent bit lines. The array consists of four identical unit cells, each containing two magnetic tunnel junctions (MTJ) and two magnetic capacitors (MC). The MTJs are labeled MTJ1, MTJ2, MTJ3, and MTJ4, and the MCs are labeled MC1 and MC2. The unit cells are arranged in a 2x2 grid. A coordinate system is shown at the bottom right, with the x-axis pointing right and the y-axis pointing up.

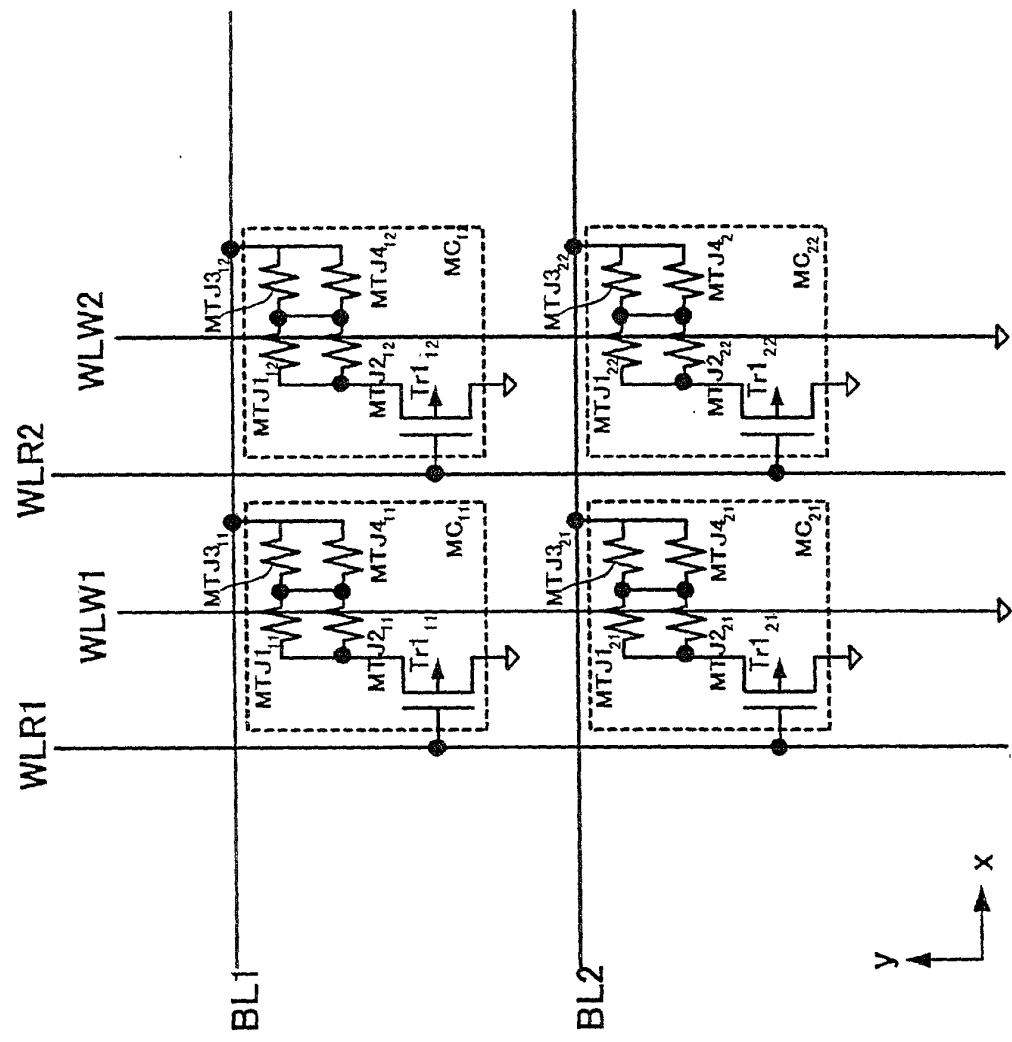


Figure 7

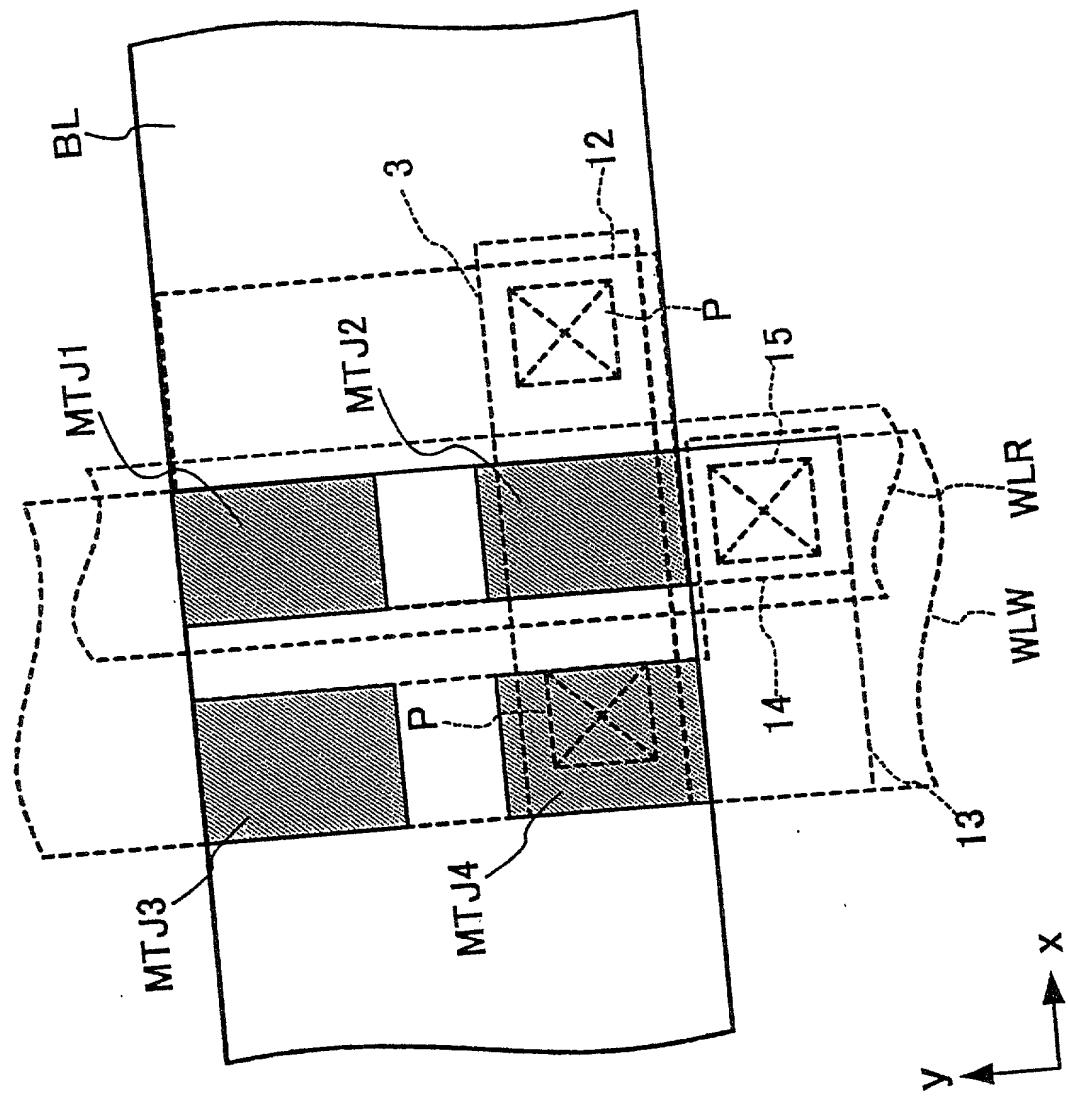


Figure 8

